

Appl. No. 10/711,877
Amdt. dated May 02, 2005
Reply to Office action of March 21, 2005

Amendments to the Drawings:

Two new sheets of drawings are added, containing Figure 8 and Figure 9 thereon. Figures 8 and 9 illustrate the reference signal circuit and the clock generator recited in claims 2, 3, 6, and 8. The specification is also amended to include explanation of these newly added figures.

5 Acceptance of the drawings is requested.

Attachment: New Sheet 2 pages

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REMARKS/ARGUMENTS

1. Rejection of claims 7, 11, 12, and 15 under 35 U.S.C. 112, second paragraph:

Claims 7, 11, 12, and 15 are rejected under 35 U.S.C. 112, second paragraph for reasons of record.

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Response:

In claim 12, the applicant has corrected the term "first reference switch" to read "first reference reset switch". No new matter has been entered.

10 According to the applicant's records of the specification and claims filed with the USPTO, claims 7, 11, and 15 each introduce the term "second feedback capacitor" as the first limitation in each claim. Therefore, antecedent basis does not need to be found in the respective preceding claims. The applicant believes that claims 7, 11, and 15 are currently in proper form with respect to 35 U.S.C. 112, second paragraph, and reconsideration of
15 claims 7, 11, 12, and 15 is respectfully requested.

2. Rejection of claims 1-15 under 35 U.S.C. 103(a):

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Yang (US 6,570,519) for reasons of record.

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Response:

Independent claims 1 and 8 are amended to overcome this rejection. Claims 1 and 8 now recite that the reset clock is out of phase with the first and second clocks. The APA does not teach the use of a reference reset switch, and therefore does not teach that a reset
25 clock controls the operation of a reference reset switch. Yang teaches a switch 302a, but does not teach that the reset clock that controls it, the first clock, and the second clock are all out of phase with each other. Yang only teaches two different phase indications Φ_1 and Φ_2 , and therefore does not teach three clocks that each out of phase with each other,

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one of which controls the reference reset switch. Since neither APA nor Yang teach this limitation, the currently amended claims 1 and 8 are patentable over the combination of APA and Yang. Claims 2-7 and 9-11 are dependent on claims 1 and 8, respectively, and should be allowed if claims 1 and 8 are allowed.

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Claim 12 contains limitations that describe the sequence of control steps taken to turn on and off the first signal input switch 33, first reference input switch 34, and the first reference reset switch 35. These three switches are controlled by three different clocks, and are not turned on and off at the same time as each other. Figure 6 illustrates the relative timings of the first clock CLK21, the second clock CLK22, and the reset clock CLKX, which control the first signal input switch 33, the first reference input switch 34, and the first reference reset switch 35, respectively. As shown in Fig.6, none of these three clock signals has the same phase as one another.

On the other hand, Yang teaches that the status of switches 302a, 302b, 304a, and 304b are always the same, and are turned on or off in unison. Yang does not teach controlling the reset switches with a clock signal that is out of phase with clock signals used to control all other switches, and therefore does not teach turning the reset switch on and off independently of other switches. Since neither Yang nor APA teach these limitations contained in claim 12, claim 12 is patentable over the combination of APA and Yang. Claims 13-15 are dependent on claim 12, and should be allowed if claim 12 is allowed.

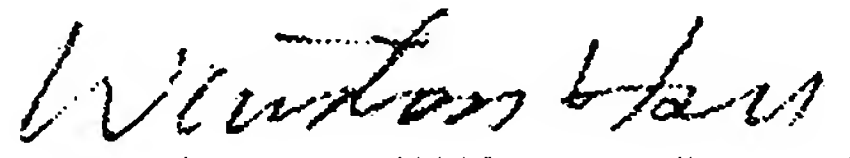
In addition to the above arguments, APA and Yang pertain to different applications, and one skilled in the art would not find it obvious to combine them to produce the claimed invention. For instance, APA applies to the field of a pipeline ADC, whereas Yang's disclosure applies to a delta-sigma modulator. Even though both APA and Yang use switches, switches are commonly used in circuit design. As Yang explains in col.4, lines 34-36, the switches 302 are used for discharging sampling capacitors Cs. However,

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in the present invention, the reset switches 35 and 45 are used to reduce the overshooting of the output signal significantly, and to increase the efficiency of the pipeline ADC.

Moreover, combining the Yang teachings with the APA in a way so as to exactly
5 produce the claimed invention is only obvious through hindsight, after having seen the present invention. One skilled in the art would not have found it obvious at the time the present invention was made to take the teachings of the APA and Yang in order to produce the claimed invention. Therefore, reconsideration of claims 1-15 is respectfully requested.

10 Respectfully submitted,



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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C.
20 is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan).

Attachments